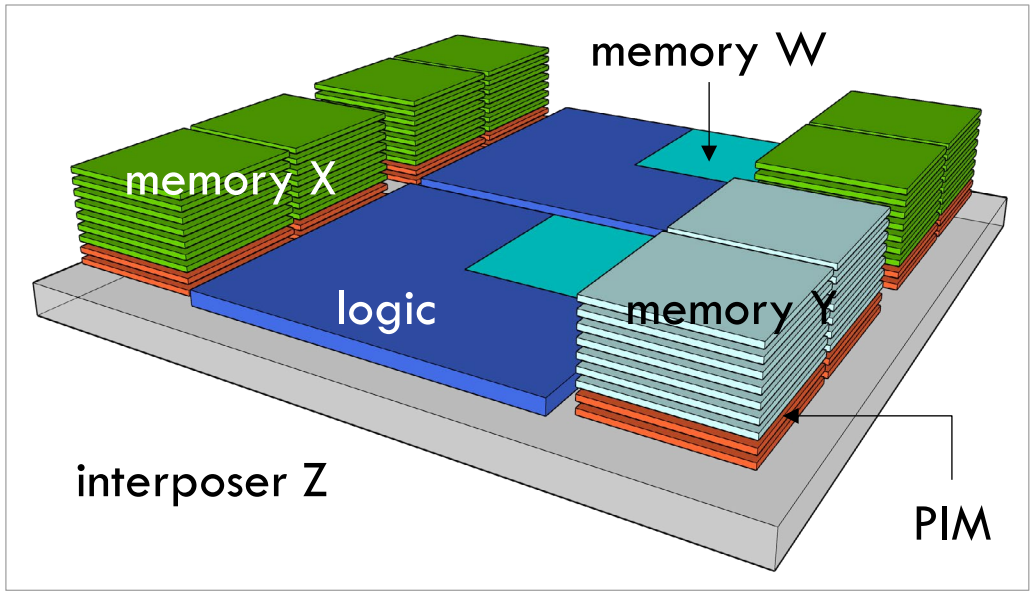


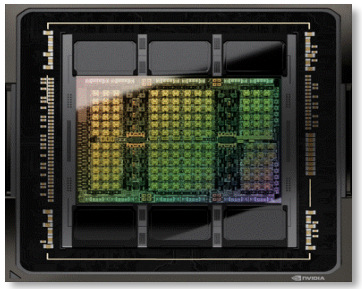
AI-DRIVEN CO-OPTIMIZATION OF DESIGN & MANUFACTURING FOR HETEROGENEOUS AI CHIPS

Sung Kyu Lim
Georgia Institute of Technology
July 3, 2025
Korea-U.S. Forum on Nanotechnology

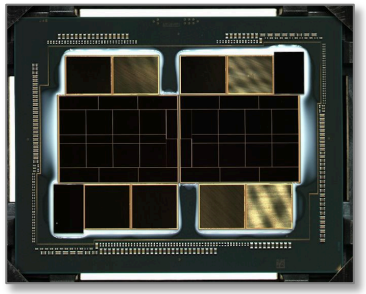
COMMERCIAL AI CHIPS: MULTI-CHIP PACKAGING

MAINSTREAM IN AI SERVICING

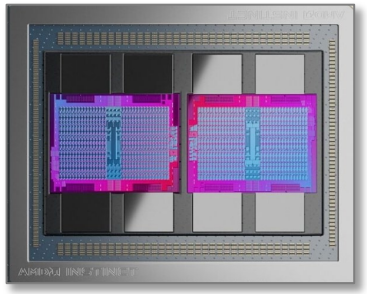
For Sale



NVIDIA

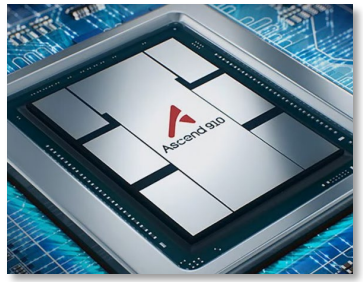


Intel



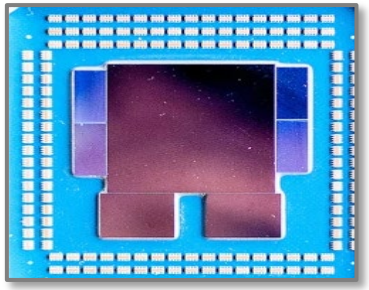
AMD

Broadcom



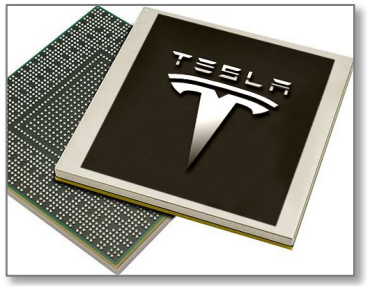
Huawei

Not for Sale



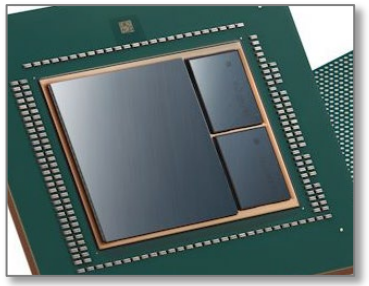
Amazon

Microsoft



Tesla

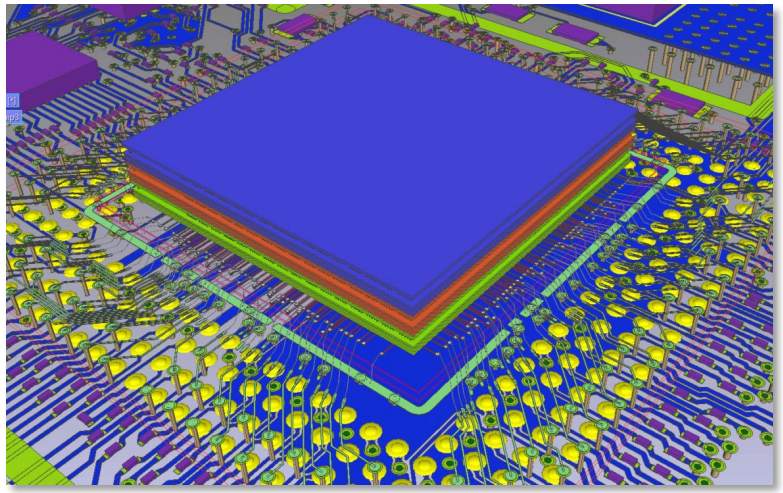
Meta



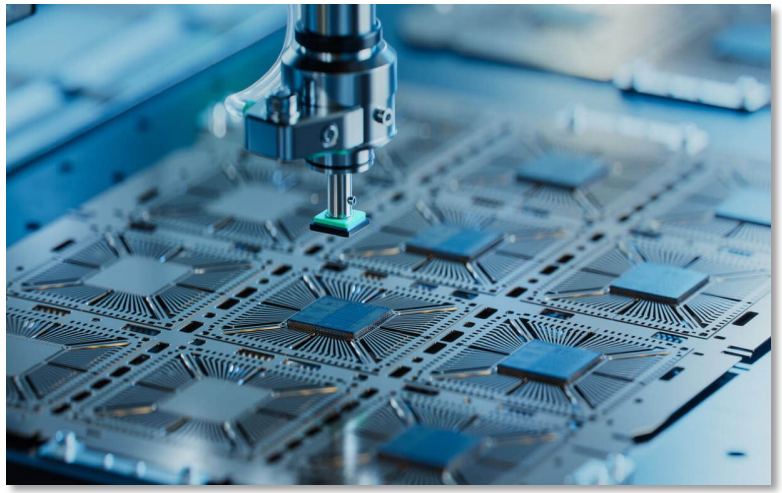
Baidu

DESIGN-MANUFACTURING CO-OPTIMIZATION

Package Design

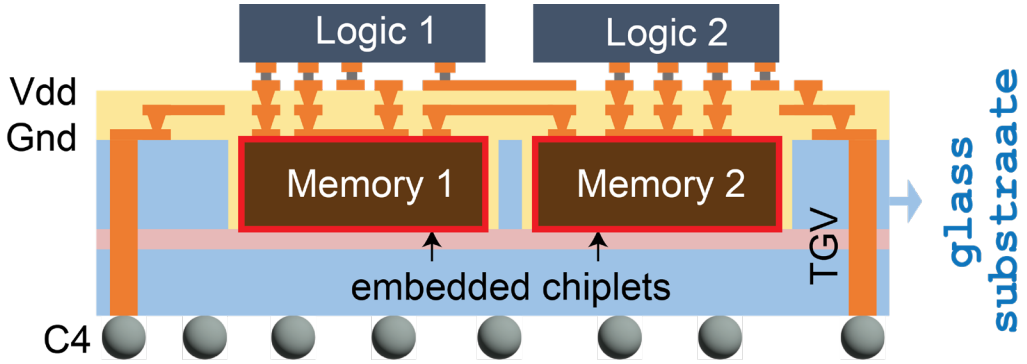


Package Manufacturing



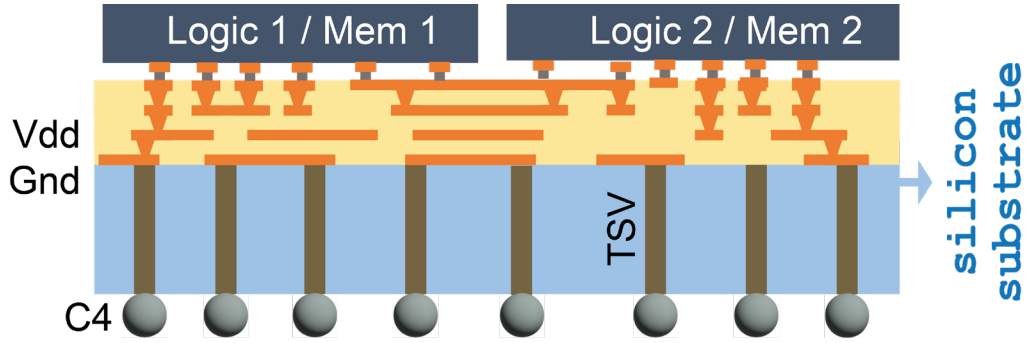
GLASS OR SILICON?

Glass Substrate



better insulation, better CTE,
larger size, lower cost, die embedding

Silicon Substrate



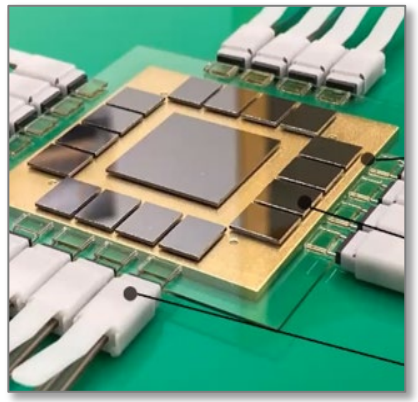
better thermal conductivity,
finer pitch interconnect

OK, but what will they do to my chips?

THREE WAYS TO ANSWER

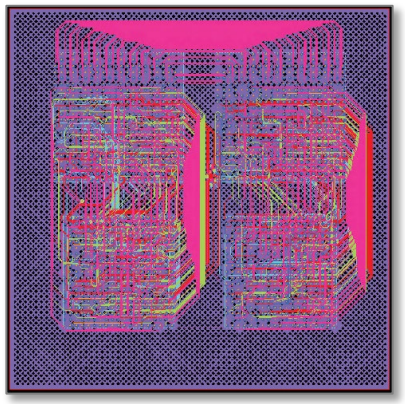
Build Samples ✗

Most accurate but
slowest & expensive



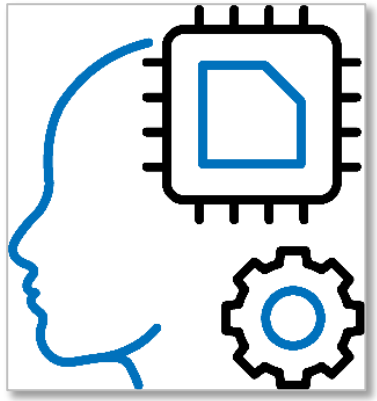
Design & Simulate ✗

Accurate but
slow



AI Prediction ✓

Fast but
inaccurate



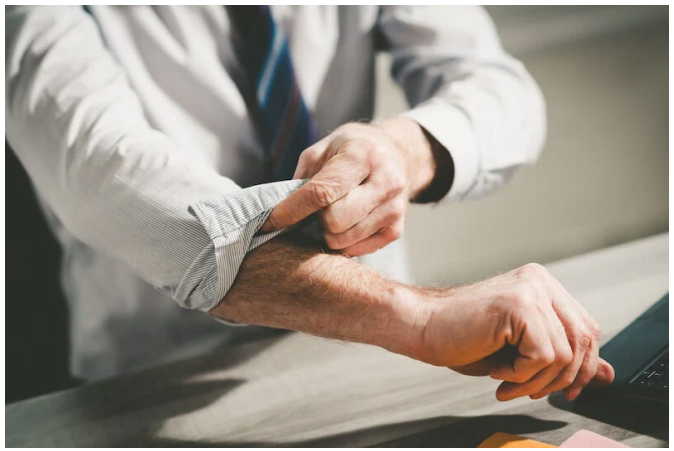
WHERE IS DATA?

2.5D IC design & simulation data

Hard to find

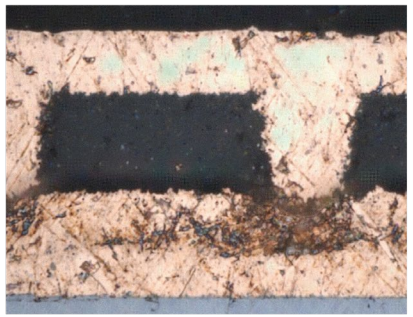
I can't wait

I will build them myself

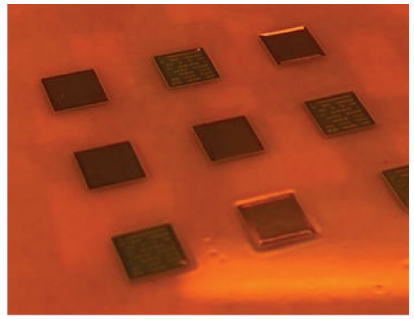


STEP 1/6: WE NEED PDK

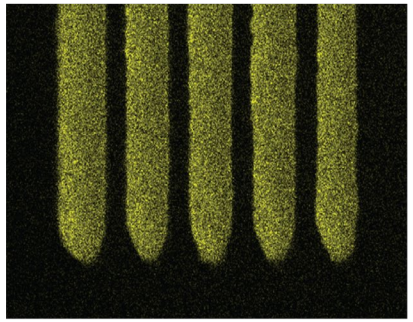
Manufacturing Samples



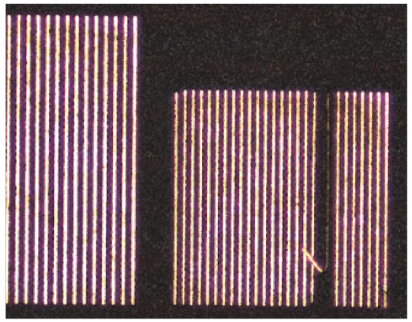
RDL via



embedded dies



through glass vias



RDL wires

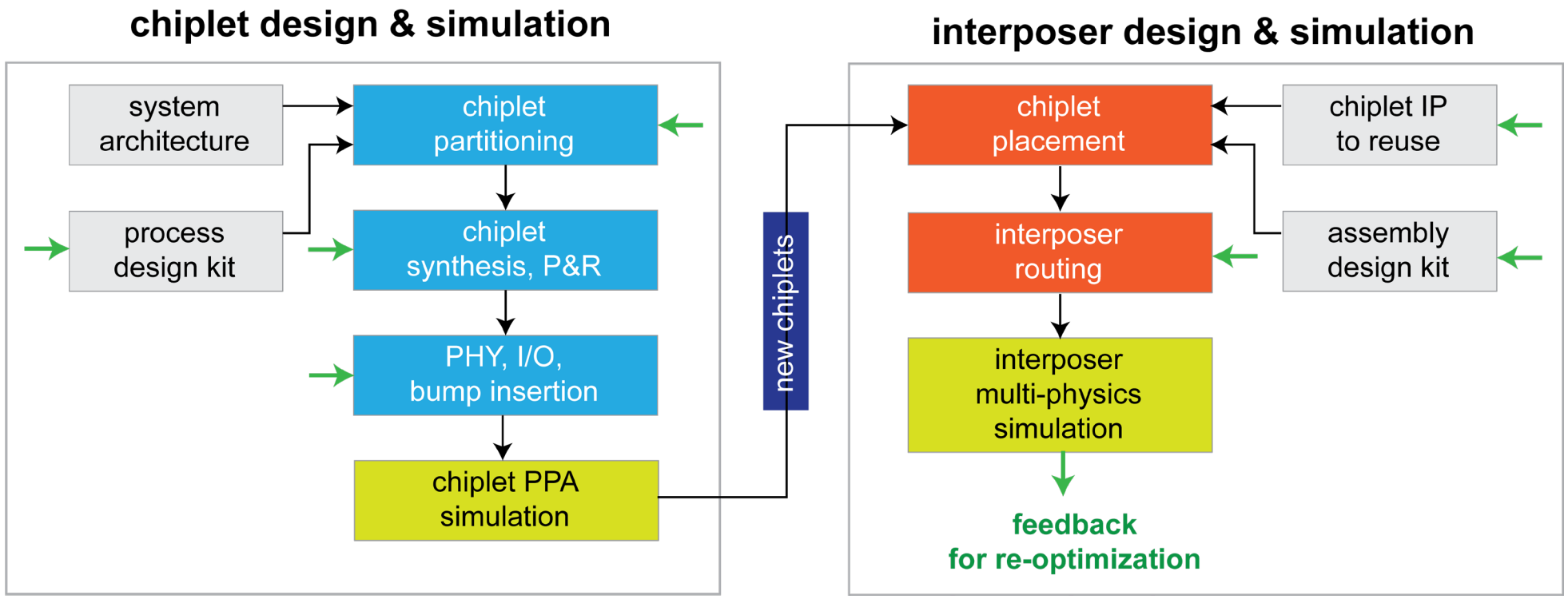
PDK Parameters

Design Rules	
Metal thickness	4um
Wire width / space	2um / 2um
Micro-bump pitch	35um

Material Properties (AGC-EN-A1)		
substrate	Permittivity (Dk)	4.9
	Young's mod (GPa)	74.8
	CTE (ppm/K)	3.2

PDK: Process Design Kit

STEP 2/6: WE NEED DESIGN TOOLS

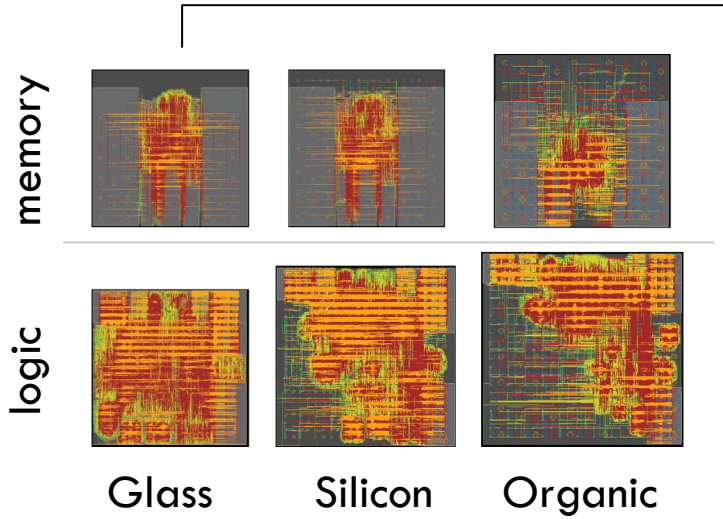


Jinwoo Kim, et al, "Architecture, Chip, and Package Co-design Flow for 2.5D IC Design Enabling Heterogeneous IP Reuse," ACM Design Automation Conference, 2019.

STEP 3/6: WE DO DESIGN

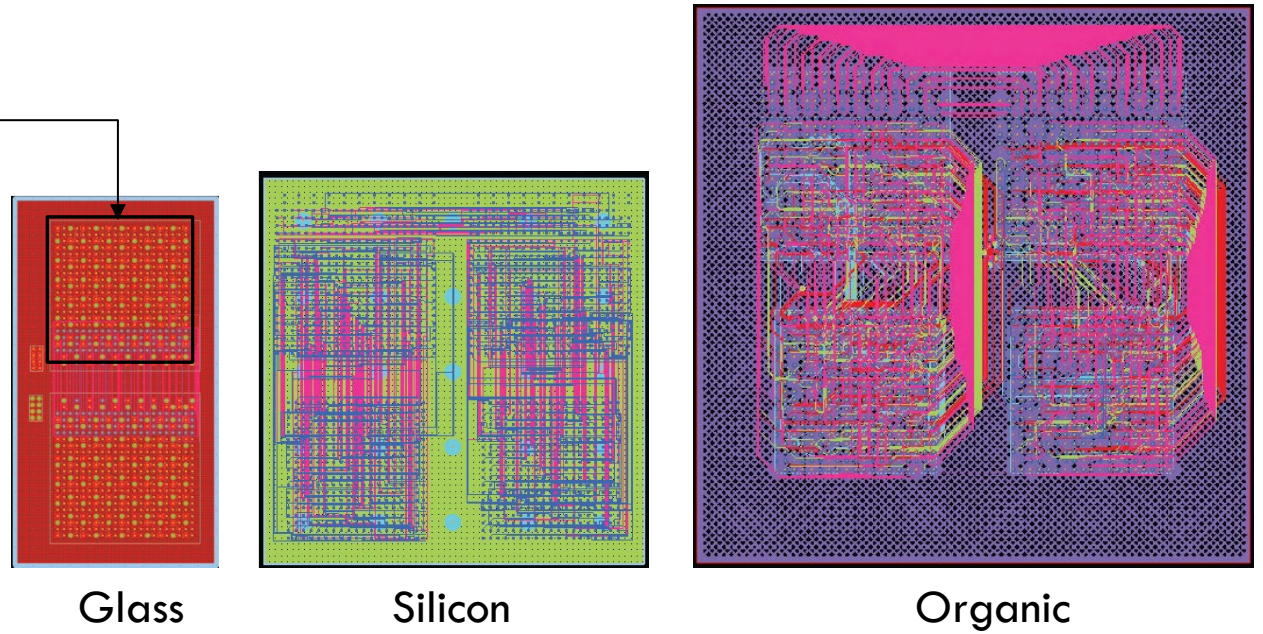
Chiplets

Multi-core RISC-V partitioned



Interposers

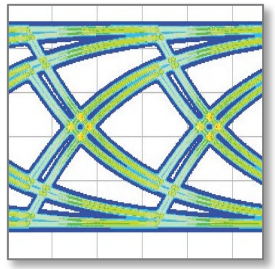
Wires, vias, bumps have high impact



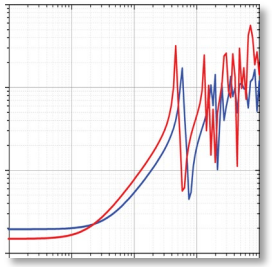
Pruek Vanna-iampikul, et al, "Glass Interposer Integration of Logic and Memory Chiplets: PPA and Signal/Power Integrity Benefits", ACM Design Automation Conference, 2023.

STEP 4/6: WE DO SIMULATION

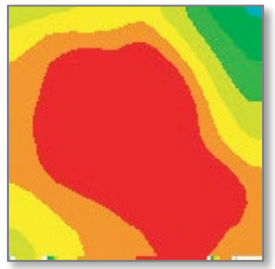
		2D	Glass	Silicon	Glass Benefit
Cost	Area (mm^2)	2.56	1.87	4.84	2.6x
	Metal layer used	-	3	4	1.3x
	Interposer WL (mm)		37.9	937	24.7x
Reliability	Eye width/height	-	1.4ns/0.8v	1.0ns/0.4V	1.4x
	PDN Impedance (Ω)		0.97	7.9	8.1x
	IVR Settling Time (us)		3.7	4.1	1.1x
	Thermal (°C)		27.5	23.3	0.8x



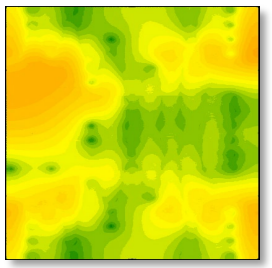
Eye diagram



PDN impedance



Thermal map

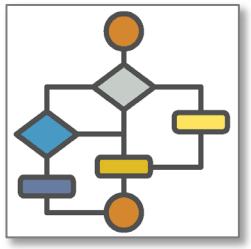


IR-drop map

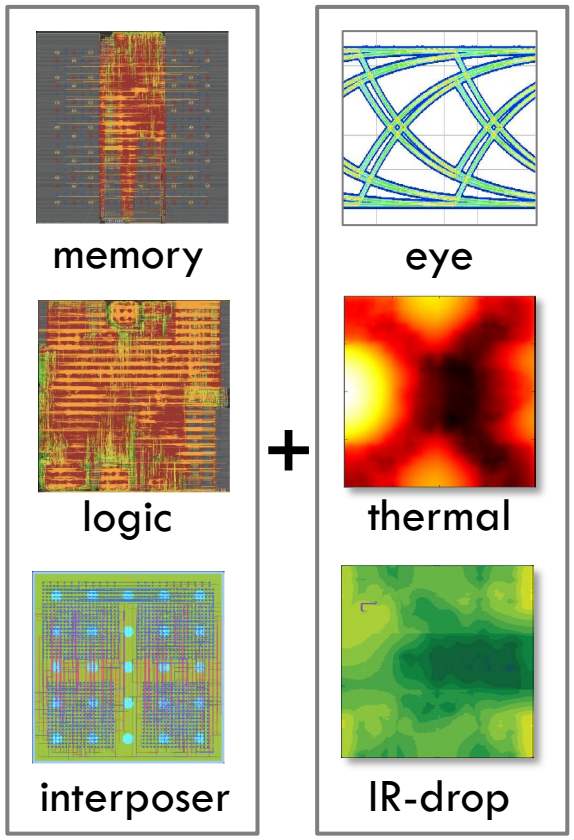
STEP 5/6: WE BUILD DATASET

design	pitch
F	X

1. Pick a pitch

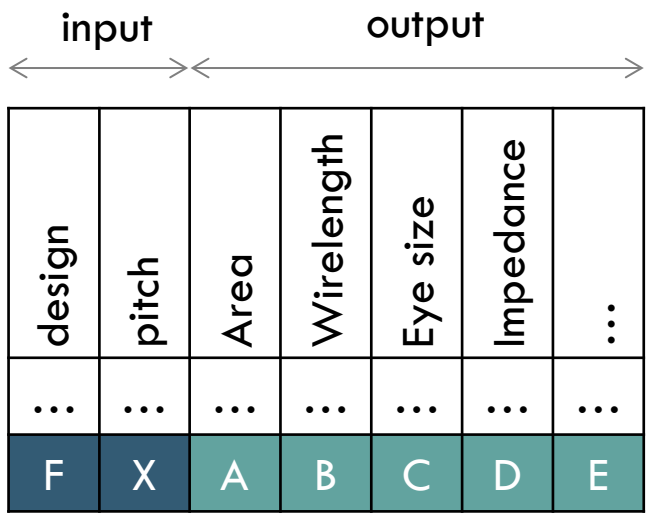


2. Run EDA flow



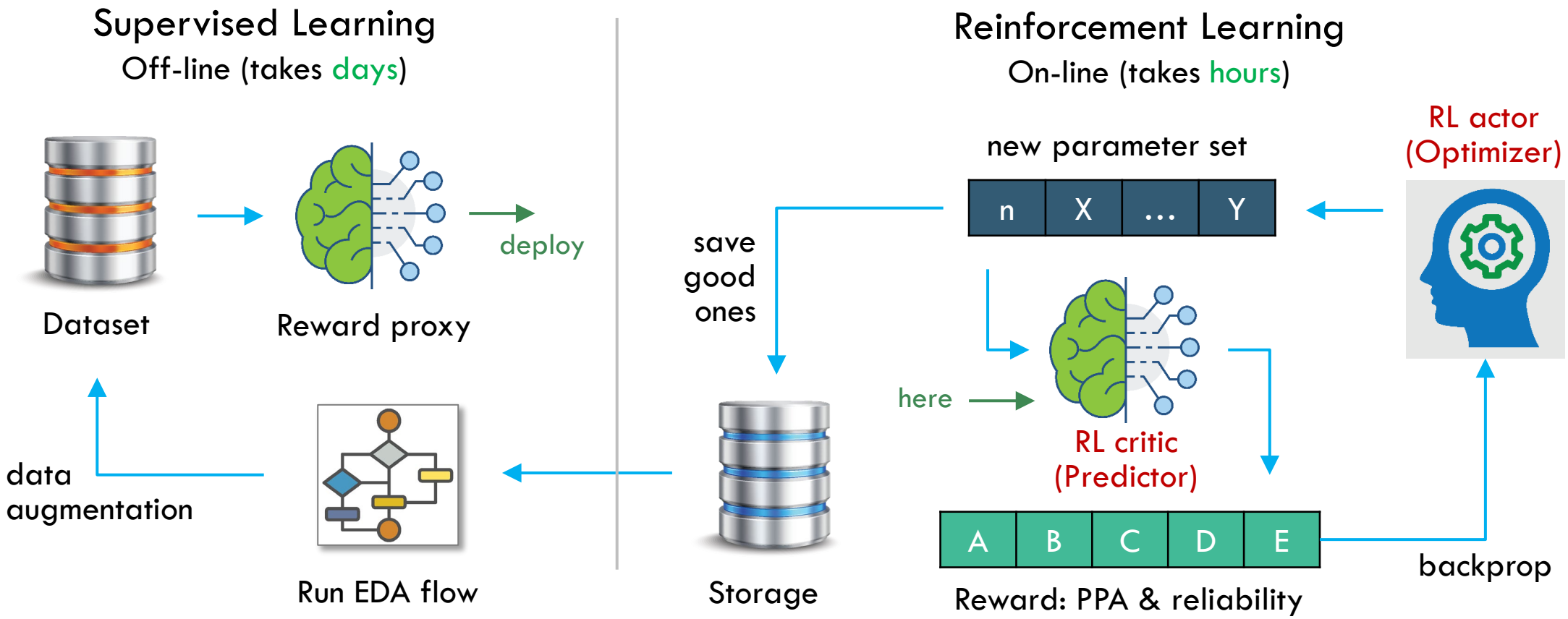
3. Obtain design & simulation results

Database: takes months



4. Add a new entry in the database

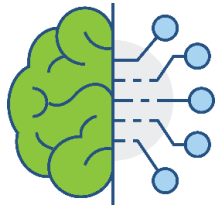
STEP 6/6: WE TRAIN AI MODELS



TWO THINGS WE ASK AI

AI Prediction
(takes seconds)

Design quality of my chip? →



design metric	prediction	accuracy
Interposer size (mm^2)	2,300	99%
Eye (ns/V)	0.32/0.89	95%
PDN impedance (Ω)	6.8	95%
Max temperature (°C)	28.0	99%

AI Optimization
(takes hours)

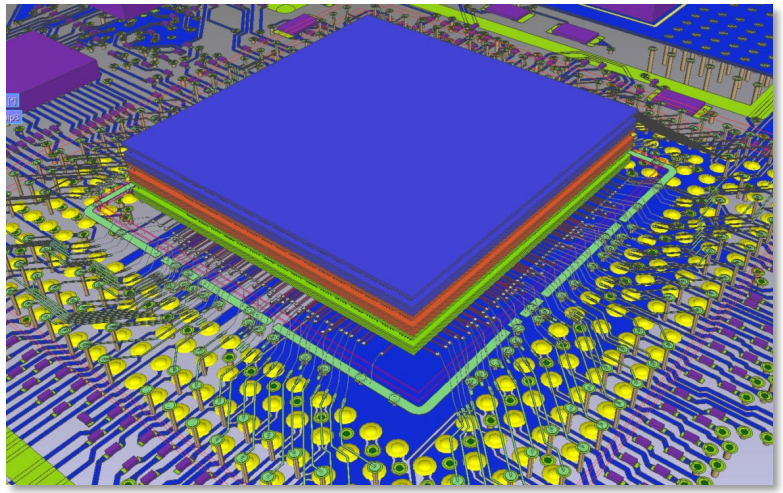
Best process recipes for my chip? →

process parameters	current	optimized
Metal thickness (um)	4	4.2
Micro-bump pitch (um)	35	36
Permittivity (Dk)	4.9	4.8
CTE (ppm/K)	3.2	3.8

Seungmin Woo, et al, "AI-Driven Evaluation and Optimization of Bump Pitch Effects on Chiplet and Interposer Design Quality", IEEE Int. Conf. on Computer-Aided Design, 2024.

MORE IMPORTANT THAN EVER

Package Design



Package Manufacturing